



09/344847

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Attorney's Docket No. S1022.80249US00

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Gajinder Singh PANESAR  
Serial No.: 09/344,847  
Filing Date: June 28, 1999  
For: DESIGN OF AN APPLICATION SPECIFIC PROCESSOR (ASP)

Patent No. 6,937,973  
Issued: August 30, 2005

Examiner: Kandasamy Thangavelu  
Art Unit: 2123

Confirmation No.: 9525

ATTN: Certificate of Correction Branch  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate**  
**SEP 15 2005**  
**of Correction**

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

- ☒ Request for Certificate of Correction
- ☒ Copies of: Pages 4-5 of 7/23/04 Amn and Col 10 of U.S. Patent No. 6,937,973
- ☒ PTO Form SB/44
- ☒ Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646-8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

## CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on September 7, 2005.

Attorney Docket No.: S1022.80429US00  
**XNDD**

Respectfully submitted,

Gajinder S. Panesar, Applicant

By   
James H. Morris  
Reg. No.: 34,681  
WOLF, GREENFIELD & SACKS, P.C.  
600 Atlantic Avenue  
Boston, Massachusetts 02210  
Tel. (617) 646-8000

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**REQUEST FOR CERTIFICATE OF CORRECTION**

Sir/Madam:

Patentee respectfully request the correction of an error found in the above-captioned patent. Specifically, there is a grammatical error in 9 of U.S. Patent No. 6,937,973 B1.

Below claim 9 as it appears in column 10, lines 40-50 of U.S. Patent No. 6,937,973.

A register definition file stored on a computer readable medium and comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the **functional** of the element and the functional status of the element, and each table further including the word location of the register within a memory map, wherein when the computer readable medium is loaded into a computer for simulating an Application Specific Processor, said register definition tables are accessed based on said word location for simulation of said registers (Emphasis added)

Below claim 9 as it appears in the amendment filed July 23, 2004.

A register definition file stored on a computer readable medium and comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the **function** of the element and the functional status of the element, and each table further including the word location of the register within a memory map, wherein when the computer readable medium is loaded into a computer for simulating an Application Specific Processor, said register definition tables are accessed based on said word location for simulation of said registers (Emphasis added)

SEP 16 2005

No amendments were made by either the Examiner or Applicant to change the word "function" to "functional" in claim 9 of issued U.S. Patent No. 6,937,973.

Support for the requested correction can be found in the enclosed, highlighted copy of pages 4-5 of the amendment filed on July 23, 2004 and column 10 of U.S. Patent No. 6,937,973. Also enclosed is PTO form SB/44.

The correction requested does not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Patentee respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

**CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)**

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on September 7, 2005.

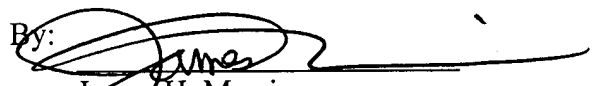


Attorney Docket No.: S1022.80429US00  
**XNDD**

Respectfully submitted,

*Gajinder S. Panesar, Applicant*

By:



James H. Morris  
Reg. No.: 34,681  
WOLF, GREENFIELD & SACKS, P.C.  
600 Atlantic Avenue  
Boston, Massachusetts 02210  
Tel. (617) 646-8000

5. (Previously presented) A computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP), wherein the computer system comprises an input means for receiving a plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure;

the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table; and

wherein the computer system further comprises an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP.

6. (Original) A computer system according to claim 5, wherein the input means comprises means for receiving a physical recording device holding the input file for each peripheral.

7. (Original) A computer system according to claim 5, wherein the output means comprises means for loading the register definition file onto a physical recording device.

8. (Currently amended) A computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file which defines in an input ~~data~~ data structure the functional attributes of a peripheral for an application specific processor in a high level language, and to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers.

9. (Previously presented) A register definition file stored on a computer readable medium and comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element,

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the function of the element and the functional status of the element, and each table further including the word location of the register within a memory map, wherein when the computer readable medium is loaded into a computer for simulating an Application Specific Processor, said register definition tables are accessed based on said word location for simulation of said registers.

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,937,973 B1  
DATED : August 30, 2005  
INVENTOR(S) : Gajinder Singh Panesar

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 9, col. 10, line 44 should read:  
--element, the **function** of the element and the functional --

MAILING ADDRESS OF SENDER

PATENT NO. 6,937,973

James H. Morris  
Wolf, Greenfield & Sacks, P.C.  
600 Atlantic Avenue  
Boston, Massachusetts 02210

SEP 16 2005